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Docket No.: T2171.0180/P180  
(PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of:

Takahisa Yamaha

Allowed: June 25, 2004

Application No.: 09/518,709 ✓

Confirmation No.: 5749

Filed: March 3, 2000

Art Unit: 2815

For: MANUFACTURE METHOD FOR  
SEMICONDUCTOR WITH SMALL  
VARIATION IN MOS THRESHOLD  
VOLTAGE

Examiner: E. Ortiz

**REQUEST FOR SUPPLEMENTAL NOTICE OF ALLOWANCE**

Attn: MS Issue Fee  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Dear Sir:

Applicants received a Notice of Allowance dated June 25, 2004.

On March 12, 2001, Applicant filed a Information Disclosure Statement. During final review of the allowed application, Applicant note that the Information Disclosure Statement of March 12, 2001 was not acknowledged.

Applicant respectfully requests that the Information Disclosure Statement dated March 12, 2001 be acknowledged and considered for the above-referenced patent application, before payment of the issue fee. A copy of said Information Disclosure Statement, Applicant's Art Citation, References submitted on 03/12/2001 (plus stamped postcard indicating receipt by the U.S. Patent Office) are enclosed for your convenience.

Application No.: 09/518,709

Docket No.: T2171.0180/P180

Please charge any credits or deficiencies to our Deposit Account No. 50-2215.

Dated: August 3, 2004

Respectfully submitted,

By 

Steven I. Weisburd

Registration No.: 27,409

DICKSTEIN SHAPIRO MORIN &  
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Attorney for Applicant



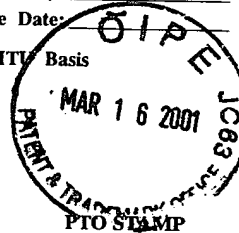
Serial No. 09/518,709 Filing Date 3-3-00 OFGS File No. P/2171-180  
Title MANUFACTURE METHOD FOR SEMICONDUCTOR ...  
First Inventor YAMAHA, T. Date 3-12-01

The PTO has received:

Last Due Date:

- ☐ Patent Application of \_\_\_\_\_  
Pages (including claims & abstract)  
☐ Declaration or ☐ Designation Sheet  
☐ Drawings \_\_\_\_\_ Sheet(s)/Figs. \_\_\_\_\_ to \_\_\_\_\_  
☐ Priority Document  
☐ Small Entity Declaration  
☐ Assignment & Conveyance Cover Sheet  
☒ Information Disclosure Statement  
☒ PTO-1449 W/4 REFS.  
☐ Amendment  
☐ Affidavit or Declaration  
☒ JP O.A./ABSTRACTS(4)

- ☐ TM Application ☐ ITU Basis  
☐ Statement of Use  
☐ Extension of Time  
☐ Notice of Appeal  
☐ Brief  
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(102)

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Our Ref.: P/2171-180

Takahisa YAMAHA

Date: March 12, 2001

Serial No.: 09/518,709

Group Art Unit: 2812

Filed: March 3, 2000

Examiner: --

For: MANUFACTURE METHOD FOR SEMICONDUCTOR WITH SMALL VARIATION IN MOS THRESHOLD VOLTAGE

Assistant Commissioner of Patents  
Washington, D.C. 20231

SUBMISSION

Sir:

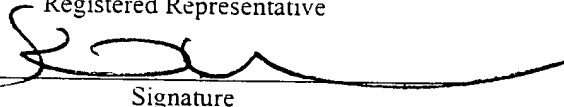
<input checked="" type="checkbox"/>	Submitted herewith is a copy of art together with an art listing form listing the same for the convenience of the Examiner.
<input checked="" type="checkbox"/>	The Japanese Publication(s) listed on the attached art listing form was/were cited in a Japanese Office Action issued in a related application. A copy of the Office Action is attached. English-language Abstracts have been provided for the references.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to:  
Assistant Commissioner of Patents, Washington, D.C. 20231, on March 12, 2001.

Respectfully submitted,

Steven I. Weisburd

Name of applicant, assignee or  
Registered Representative



Signature  
March 12, 2001  
Date of Signature



Steven I. Weisburd

Registration No.: 27,409

OSTROLENK, FABER, GERB & SOFFEN, LLP

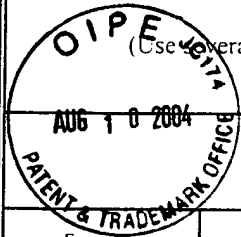
1180 Avenue of the Americas

New York, New York 10036-8403

Telephone: (212) 382-0700

SIW:sks/Enclosures

Group Art Unit --



Examiner Initials	Document Number								Date	Name	Class	Sub- class	Filing Date If Appropriate

[illegible]

		Japanese Office Action issued July 4, 2000.

Date Considered

00499068.1

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